REMARKS

Claims 1-74 are currently pending in the application; claims 3, 4, 6, 8-10, 12, 15, 16, 18, 20-22, 24, 26-30, 32-34, 36-54, 56-71 and 73 are withdrawn from consideration. Claim 55 has been amended. Support for the amendments is found, for example, from Page 29, Paragraph 3 to Page 30, Paragraph 2 of the specification and Figures 9 and 10 of the drawings. No new matter is introduced by the amendment.

Initially, Applicants would like to thank the Examiner for the indication that claims 13, 14, 17, 19, 23, 25, 31, 35 and 74 are allowable. The Examiner has objected to claims 11 and 68 as being dependent upon a rejected base claim, but indicated that the claims would be allowable if rewritten in independent form including all of the limitations of any intervening claims.

The Examiner has rejected claims 1, 55 and 72 under 35 U.S.C. § 102(e) as allegedly anticipated by U.S. Patent No. 6,383,916 issued to Lin (hereinafter "Lin"). Applicants respectfully submit the rejection is overcome in view of the remarks made herein.

To maintain a claim rejection under 35 U.S.C. § 102, a prior art reference must disclose each and every element of the claim. Lin fails to do so.

Independent claim 1 recites a semiconductor unit having two device terminals for every one input/output signal. The semiconductor unit comprises a laminated substrate and a semiconductor chip. The substrate comprises at least two wiring layers, which include a signal wiring layer and a power-supply or ground wiring layer. The substrate has a main surface. The semiconductor chip has an input/output pad and is mounted on the main surface of the laminated substrate through the input/output pad. Significantly, the two device terminals are mounted on the laminated substrate and connected to both ends of a signal wire in the signal wiring layer, and the signal wire is connected to the input/output pad of the semiconductor chip through a via hole. Thus, the invention as recited claim 1 contemplates a novel semiconductor configuration wherein

two terminals are connected to a wire in a wiring layer and the wire is further connected to the pad through a via hole, as illustrated in Fig. 6 of the application.

Lin discloses a method for forming a top metallization system for high performance integrated circuits, and a semiconductor structure formed by the method. Specifically, the Lin semiconductor structure is used to "elevate or fan-out the fine-line interconnects and to remove these interconnects from the micro and sub-micro level to a metal interconnect level that has considerable larger dimensions and is therefore with smaller resistance and capacitance and is easier and more cost effective to manufacture" (see Col. 6, Lines 49-54). Lin discloses a semiconductor structure, as shown from Figs. 1-8 thereof including a plurality of signal pads 6 (contact points in micro and sub-micro level) connected to a plurality of contact pads 10 (metal level pads) through a via 7. However, Figs. 1-8 and the corresponding description thereof only disclose that a signal pad is connected to a contact pad through a via.

As illustrated in Figs. 9-11, Lin further extends the above designing concept to BGA (Ball Grid Array) chips by connecting the relatively crowded and smaller contact balls at the chip side to the relatively loosely distributed and bigger contact balls at the substrate side through wires disposed in the substrate, thereby "the BGA pads can be arranged in a different and arbitrary sequence that is required for further circuit design or packaging" (see Col. 8, Lines 14-16 of Lin). However, Figs. 9-11 and the corresponding description thereof only disclose that two contact balls are connected with each other through a wire.

In contrast, claim 1 recites that the two device terminals are connected to both ends of a signal wire, and the signal wire is connected to the input/output pad of the semiconductor chip through a via hole. Neither the semiconductor structure shown in Figs. 1-8 of Lin nor the semiconductor structure shown in Figs. 9-11 of Lin disclose the above feature recited by claim 1.

In fact, the Examiner has improperly combined the two semiconductor structures of Lin to arrive at the combination of features recited by claim 1. Similarly, concerning independent claims 60 and 61 reciting that the two device terminals are connected to each other through a via hole and the via hole is connected to the input/output pad of the semiconductor chip through a wire, Lin also fails to disclose this feature based on the above discussion.

Independent claim 55 recites, *inter alia*, "said two device terminals being connected to each other through a wire and the wire being further connected to an input/output pad of a semiconductor chip that corresponds to said input/output signal through another wire". As discussed above, Lin discloses by Figs. 1-8 thereof and the corresponding description a semiconductor structure having two contact balls connected with each other through a wire. Lin further discloses by Figs. 9-11 and corresponding description a semiconductor structure having a signal pad connected to a contact pad through a via. However, neither of the semiconductor structures disclosed by Lin teach or suggest that two device terminals are connected to each other through a wire and the wire is further connected to an input/output pad of a semiconductor chip that corresponds to said input/output signal through another wire, as recited by claim 55.

Independent claim 72 is directed to a semiconductor unit comprising a semiconductor chip having an input/output pad and a package having a main surface and a back surface. The package comprises at least two ball terminal adhesive areas for every single input/output signal on the main and back surfaces of the package. A ball terminal is adhered to only one ball terminal adhesive area on one surface of the package. The chip pads formed by the two ball terminal adhesive areas make it possible for ease of suitable wiring layouts. Significantly, the two ball terminal adhesive areas are connected to each other through a via hole or a wire, and the via hole or wire is connected to the input/output pad the semiconductor chip through a wire. As discussed above, Lin discloses

by Figs. 1-8 thereof and the corresponding description a semiconductor structure having two contact balls connected with each other through a wire. Lin further discloses by Figs. 9-11 and corresponding description a semiconductor structure having a signal pad connected to a contact pad through a via. However, neither of the semiconductor structures disclosed by Lin teach or suggest that two terminal adhesive areas are connected to each other through a via or wire and the via or wire is further connected to an input/output pad of a semiconductor chip through a wire, as recited by claim 77.

Therefore, Lin fails to disclose each and every element of claims 1, 55 and 72. Accordingly, the rejection of claims 1, 55 and 72 under 35 U.S.C. § 102(e) based on Lin is overcome and withdrawal thereof is respectfully requested.

The Examiner has rejected claims 2 and 61 under 35 U.S.C. § 103(a) as being unpatentable over Lin in view of U.S. Patent No. 6,137,164 issued to Yew et al., (hereinafter "Yew"). Applicants respectfully submit the rejection is overcome in view of the remarks made herein.

Independent claim 1, from which claim 2 depends, is discussed above. Lin is discussed above relative to claim 1.

Independent claim 61 recites a semiconductor unit having two device terminals for every one input/output signal. The semiconductor unit comprises a laminated substrate and two semiconductor chips. The substrate comprises at least two wiring layers including a signal wiring layer and a power-supply or ground wiring layer. The substrate has a main surface and a back surface. The semiconductor chips each have an input/output pad and are mounted on the main surface and the back surface of the laminated substrate, respectively. The two device terminals are disposed on the main surface and the back surface of the laminated substrate opposite to each other. Significantly, the two device terminals are connected to each other through a via hole, while

the via hole is connected to the input/output pads of the semiconductor chip through a wire (a configuration wherein the two terminals are connected through a via hole and the via hole is wired to the pads, see Figs.26B and 26C). As discussed above, Lin discloses by Figs. 1-8 thereof and the corresponding description a semiconductor structure having two contact balls connected with each other through a wire. Lin further discloses by Figs. 9-11 and corresponding description a semiconductor structure having a signal pad connected to a contact pad through a via. However, neither of the semiconductor structures disclosed by Lin teach or suggest that two device terminals are connected to each other through a via and the via is further connected to an input/output pad of a semiconductor chip through a wire, as recited by claim 61.

Yew discloses an assembly for stacking IC devices. Yew is relied on to allegedly teach a substrate having two semiconductor chips mounted on the main surface and back surface respectively. However, Yew fails to overcome the underlying deficiencies identified in Lin. Therefore, Lin and Yew, taken alone or in any proper combination, fail to disclose or suggest the combination of features, as recited in Claims 2 and 61. Accordingly, the rejection of claims 2 and 61 under 35 U.S.C. § 103(a) over Lin in view of Yew is overcome and withdrawal thereof is respectfully requested.

The Examiner has rejected claim 5 under 35 U.S.C. § 103(a) as unpatentable over Yew in view of U.S. Patent No. 6,630,628 issued to Devnan et al., (hereinafter "Devnan"). Applicants respectfully submit the rejection is overcome in view of the remarks made herein.

Independent claim 1, from which claim 5 depends, is discussed above. Yew is discussed above.

As shown above, Yew fails to disclose or suggest that two device terminals for every one input/output signal are mutually connected to each other through a signal wire or a via hole, and

the signal wire or via hole is further connected to an input/output pad of a semiconductor chip through a via hole or a signal wire.

Devnan discloses a high-performance laminate for integrated circuit interconnection. Likewise, Devnan fails to disclose the above features, thus cannot overcome the underlying deficiencies identified in Yew. Therefore, Yew and Devnan, taken alone or in any proper combination, fail to disclose or suggest the combination of features, as recited in claim 1, from which claim 5 depends. Accordingly, the rejection of claim 5 under 35 U.S.C. § 103(a) over Yew in view of Devnan is overcome and withdrawal thereof is respectfully requested.

The Examiner has further rejected claims 7 and 60 under 35 U.S.C. § 103(a) as unpatentable over Lin in view of U.S. Patent No. 6,184,477 issued to Tanahashi ("Tanahashi"). Applicants respectfully submit the rejection is overcome in view of the remarks made herein.

Independent claim 1, from which claim 7 depends, is discussed above. Lin is discussed above relative to claim 1.

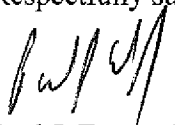
Independent claim 60 recites a semiconductor unit having two device terminals for every one input/output signal. The semiconductor unit comprises a laminated substrate and a semiconductor chip. The substrate comprises at least two wiring layers, which include a signal wiring layer and a power-supply or ground wiring layer. The substrate has a main surface and a back surface. The semiconductor chip has an input/output pad and is mounted on the main surface of the laminated substrate. The two device terminals are disposed on the main surface and the back surface of the laminated substrate opposite to each other. Significantly, the two device terminals are connected to each other through a via hole, while the via hole is connected to the input/output pad of the semiconductor chip through a wire (a configuration wherein the two terminals are connected through a via hole and the via hole is wired to the pad, see Figs.23A and 23B). As

discussed above, Lin discloses by Figs. 1-8 thereof and the corresponding description a semiconductor structure having two contact balls connected with each other through a wire. Lin further discloses by Figs. 9-11 and corresponding description a semiconductor structure having a signal pad connected to a contact pad through a via. However, neither of the semiconductor structures disclosed by Lin teach or suggest that two device terminals are connected to each other through a via and the via is further connected to an input/output pad of a semiconductor chip through a wire, as recited by claim 60.

Tanahashi discloses a multi-layer circuit substrate having orthogonal grid ground and power planes. Tanahashi is relied on to allegedly teach or suggest a signal layer between a power layer and a ground layer, the signal layer forming a strip line. Tanahashi fails to overcome the underlying deficiencies identified in Lin. Therefore, Lin and Tanahashi, taken alone or in combination, fail to disclose or suggest the combination of features of claims 7 and 60. Accordingly, the rejection of claims 7 and 60 under 35 U.S.C. § 103(a) over Lin in view of Tanahashi is overcome and withdrawal thereof is respectfully requested.

In view of the foregoing amendments and remarks, it is respectfully submitted that all claims presently pending in the application are believed to be in condition for allowance, which action is earnestly solicited.

Respectfully submitted,



Paul J. Esatto, Jr.
Registration No. 30,749

Scully, Scott, Murphy & Presser, P.C.
400 Garden City Plaza, Suite 300
Garden City, New York 11530
(516) 742-4343
PJE/HC:me